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TITLE: Massively parallel diagonal fold tree array processor - with processors containing instruction and data storage units, and receiving and executing instructions

INVENTOR: DELGADO-FRIAS, J G ; PECHANЕК, G G ; VASSILIADIS, S

PATENT-ASSIGNEE:

ASSIGNEE

CODE

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IBMC

PRIORITY-DATA: 1992US-0881597 (May 12, 1992), 1994US-0359250 (December 19, 1994), 1995US-0415775 (March 30, 1995)

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PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
<input type="checkbox"/> EP 569763 A2	November 18, 1993	E	022	G06F015/80
<input type="checkbox"/> US 5784632 A	July 21, 1998		000	G06F015/00
<input type="checkbox"/> EP 569763 A3	July 13, 1994		000	G06F015/80
<input type="checkbox"/> US 5682544 A	October 28, 1997		018	G06F015/18

DESIGNATED-STATES: DE FR GB

CITED-DOCUMENTS: No-SR. Pub; 2. Jnl. Ref ; GB 2219106 ; US 4514807 ; US 4942517 ; WO 9118351

APPLICATION-DATA:

PUB-NO	APPL-DATE	APPL-NO	DESCRIPTOR
EP 569763A2	April 26, 1993	1993EP-0106730	
US 5784632A	May 12, 1992	1992US-0881597	Cont of
US 5784632A	March 30, 1995	1995US-0415775	
EP 569763A3	April 26, 1993	1993EP-0106730	
US 5682544A	May 12, 1992	1992US-0881597	Div ex
US 5682544A	December 19, 1994	1994US-0359250	

INT-CL (IPC): G06F 15/00; G06F 15/18; G06F 15/80

ABSTRACTED-PUB-NO: EP 569763A

BASIC-ABSTRACT:

The system includes root tree processors, communicating ALU trees and processing elements (PEs). A communication component communicates both instructions and data between the root tree processors and the processing elements.

Each processor contains instruction and data storage units, receives instructions and data and executes instructions. One embodiment further includes N^2 processing elements, placed in the form of an N by N matrix and identified with a two subscript notation $PE_{\text{column}, \text{row}}$ that has been folded along the diagonal and made up of diagonal cells and general cells.

USE - Modelling highly computational parallel data algorithms, eg matrix processing and high connectivity neural networks.

ABSTRACTED-PUB-NO:

US 5682544A

EQUIVALENT-ABSTRACTS:

A computer system apparatus comprising:

root tree processors;

communicating ALU trees coupled to the root tree processors;

processing elements (PEs) coupled to the communicating ALU trees;

means coupled to the root tree processors and the processing elements, for communicating both instructions and data between the root tree processors and the processing elements;

wherein each PE contains instruction and data storage units, receives instructions and data, and execute instructions, wherein there are N^2 PEs, N communicating ALU trees, and N root tree processors for a N array structure where N is a positive integer; and

wherein each communicating ALU tree connects to N PEs at leaf nodes of the tree and one root tree processor which connects to a root of the tree providing results to a Host interface and where said communicating ALU trees, PEs, and root tree processors constituting the N array structure include:

means coupled to each PE for inputting tagged instructions and data values to the PEs from the root tree processors through the communicating ALU trees's path,

said root tree processor coupled to each PE controlling input of instructions and data in each PE,

means in each PE for the execution of the received instructions in each PE,

means in each PE for the execution, in an auto mode, of a previously received instruction when data is received to be used in a next operation,

instruction decode means in each PE for operand selection and destination path control to selectively store results locally in each PE or to send results to the attached communicating ALU tree,

means in each PE for converged function execution of values received from multiple PEs, and

host interface means coupled to each root tree processor for inputting of external data values to each root tree processor.

US 5784632A

The system includes root tree processors, communicating ALU trees and processing elements (PEs). A communication component communicates both instructions and data between the root tree processors and the processing elements.

Each processor contains instruction and data storage units, receives instructions and data and executes instructions. One embodiment further includes N2 processing elements, placed in the form of an N by N matrix and identified with a two subscript notation PEcolumn,row that has been folded along the diagonal and made up of diagonal cells and general cells.

USE - Modelling highly computational parallel data algorithms, eg matrix processing and high connectivity neural networks.

CHOSEN-DRAWING: Dwg.3a-c/7 Dwg.5a/7

TITLE-TERMS: PARALLEL DIAGONAL FOLD TREE ARRAY PROCESSOR PROCESSOR CONTAIN
INSTRUCTION DATA STORAGE UNIT RECEIVE EXECUTE INSTRUCTION

ADDL-INDEXING-TERMS:
Tera Computer

DERWENT-CLASS: T01

EPI-CODES: T01-M02C1;

SECONDARY-ACC-NO:
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